

# Thin Film Ceramic Substrate Design Guide

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## **Section 1: Scope**

### **1.1: Purpose**

This document is intended to provide a guide to designers of thin film substrates. The guide is intended to document the substrate features that can be reliably and economically fabricated in Tecdia's Hybrid Ceramic Technology Group (HCT) based in Cebu Philippines. In many cases, the limits stated herein represent features that have been successfully produced in the past, rather than a fundamental limit on the capabilities of a given process. As more definitive data is obtained on the processes, the procedure will be updated accordingly.

If a designer is able to produce a working design within the limits of this document, he can count on obtaining quality substrates. If the particular needs of a given design fall outside of these limits, the designer should discuss these methods with Tecdia personnel. It may be possible for Tecdia to develop a new process or refine an existing process to achieve the desired results. It also may be decided that the existing processes can support the design even with low yields.

### **1.2: Applicability**

This design guideline manual only applies to thin film ceramic substrates made by the Tecdia thin film ceramic substrate group based in Cebu Philippines.

### **1.3: Applicable Documents**

Tecdia Visual Inspection Criteria Document

Tecdia QA screening Document

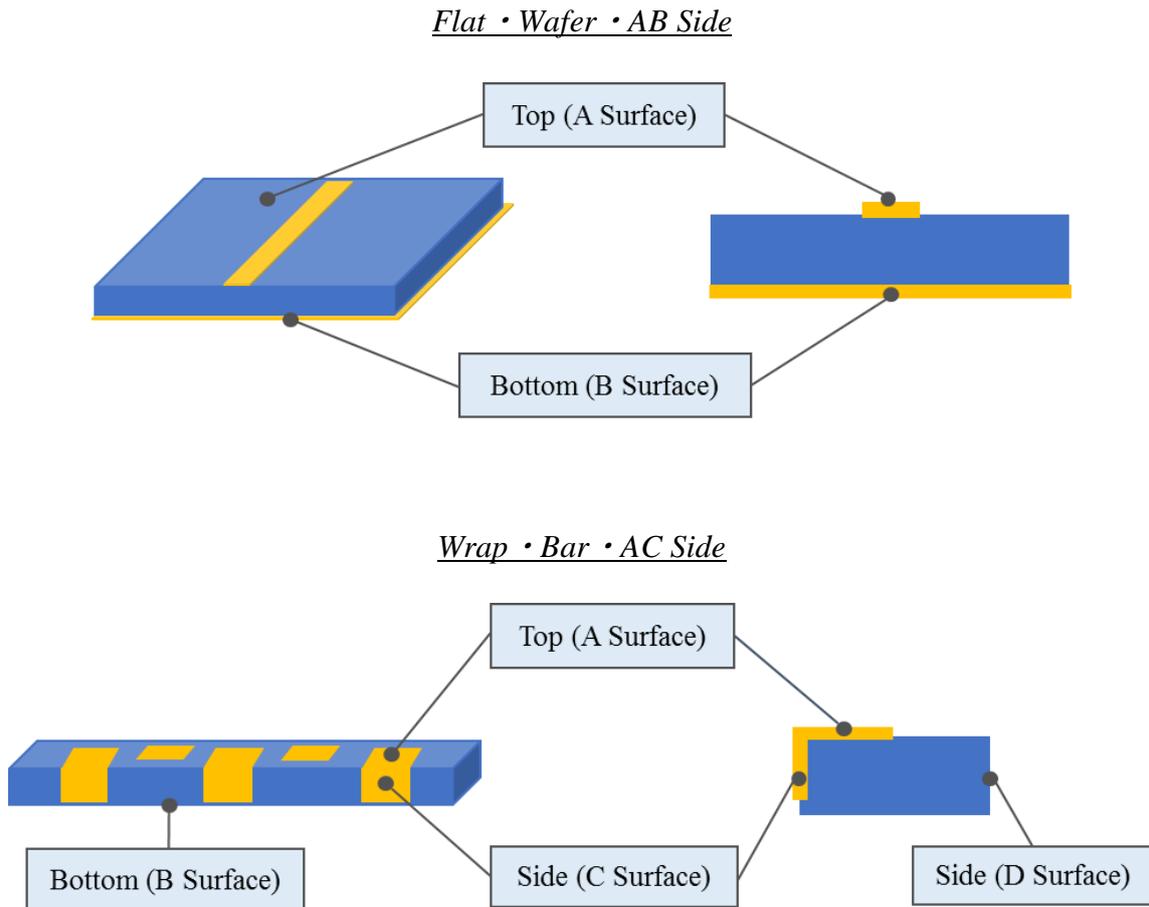
MIL-STD-883: Test Method Standard Microcircuits

## Section 2: Introduction to Ceramic Substrates

### 2.1: Surface Reference

Please reference FIG 2.1.1 for Tecdia's surface reference method for both "flat" and "wrapped" designs.

FIG 2.1.1: Surface Reference Methods



### 2.2: Useful Vocabulary

*Substrate:* A substance or layer that underlies something, or on which some process occurs, such as a ceramic.

*As Fired:* A substrate surface condition where the surface receives no treatment after sintering.

*Lap and Polish:* The processes used to grind and smooth the surface of a substrate after sintering.

*Metallization Layer:* The layers of metallization applied to the surface of the substrate.

Table 2.2.1: Metallization Stack

Metallization Layer	Applicable Metals	Purpose
Seed Layer / Adhesion Layer	Ti	Create strong bond between metal and ceramic
Barrier Layer	Pt	An optional metallization layer that protects covered layers from unwanted embrittlement and diffusion from other metals in the metallization stack. Barrier layers usually sit between the seed layer and the conductor layer or between the conductor layer and the solder layer.
Conductive Layer	Au	Wire bondable (Au only), A high current density conductive layer for passing DC and AC Current.

*Solder Barrier:* A barrier layer placed to prevent diffusion of solder into another metallization layer.

*Wrap:* Metallization connected over the edge of a substrate.



*Laser Machining:* Laser drilling and cutting performed on the ceramic to creates holes and cut outs

*Cut out:* A laser machined feature in the substrate with no metallization on the inside walls.

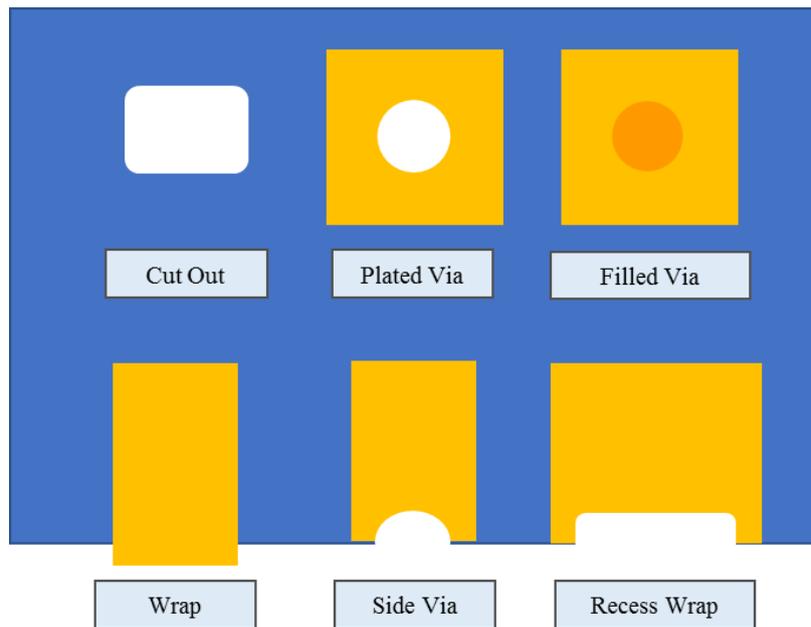
*Plated Via:* A hole with metallization on the inside walls that creates an electrical connection from the top side to the bottom side of the substrate.

*Filled Via:* A plated via hole plugged with some material to prevent solder creep up or increase thermal conductivity.

*Side Via:* A plated via made at the edge of the substrate

*Recess Wrap:* A wrap made with a recess in the substrate that allows the wrap to be made with a more efficient Post-Cut Laser machining process.

Fig 2.2.1: Wraps and Laser Machined Features



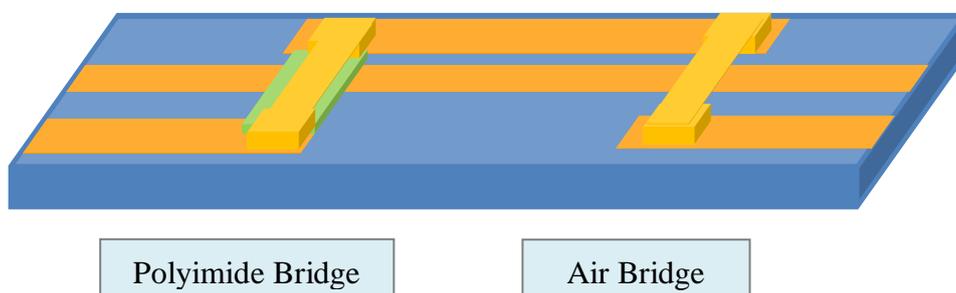
*Preform Solder:* Solder blocks placed and reflowed to attach substrate and component

*Pre-deposited AuSn Solder:* Solder pads that are applied to components and substrates through various deposition methods such as electroplating, evaporation and sputtering.

*Air Bridge:* A bridge created in the conductor layer that allows to traces to cross without connecting. Airbridges have no dielectric sitting between the overlapping conductors.

*Polyimide Bridge:* A bridge created in the conductor layer that allows to traces to cross without connecting. Polyimide Bridges have polyimide sitting between the overlapping conductors.

Fig 2.2.2: Bridges



*Solder Dam:* A structure created in the circuit to prevent solder from spreading during reflow.

*TaN / Resistor:* Thin Film Resistor structure made from Tantalum Nitride (TaN)

## Section 3: Circuit Order Requirements

### 3.1: Required Information for Quote

Non-CAD Files such as .PDF, .JPEG and .GIF can be sent for quoting only. Production/sample requests require CAD files. In order to quote along a drawing with easily recognizable structures and the information in Table 3.1.1, when applicable, must be provided.

Table 3.1.1: Required Information for Quote

Specification	Example
Substrate Material	Alumina (Al <sub>2</sub> O <sub>3</sub> ) 99.6%
Surface Finish	Polished: 0.025 $\mu$ m Ra Max.
Substrate Thickness with Tolerance	0.254 $\pm$ 0.025 mm
Chip Size with Tolerance	1 $\pm$ 0.05 X 1 $\pm$ 0.05 mm
Metallization Stack with Au Thickness and Tolerance	Ti-Pt-Au (1 $\mu$ m Min)
Required Pattern to Pattern Tolerance	$\pm$ 25 $\mu$ m
Line and Space Tolerance	$\pm$ 25 $\mu$ m
TaN Sheet Resistance	50 $\Omega$ / $\square$
Tan Resistor Tolerance	$\pm$ 20%
AuSn Mixture with Tolerance	Au 80% $\pm$ 10%/Sn 20% $\pm$ 10%
AuSn Thickness with Tolerance	5 $\pm$ 2 $\mu$ m
Via Diameter	0.2 mm
Via/ Cut Out Location Tolerance	$\pm$ 50 $\mu$ m
Via Diameter Tolerance	$\pm$ 25 $\mu$ m
Quantity to quote	MOQ, 100 pcs & 500 pcs

### 3.2: Required CAD File Format

Please consider the following rules when preparing and sending CAD files for Tecdia's substrate group. CAD files are required for mask production.

1. AutoCAD .DWG or .DXF files only. Other CAD extensions such as Gerber and GDS require conversions that can lead to errors and misinterpretations of the drawing.
2. AutoCAD .DWG or .DXF file extensions are preferred however, we can also accept any programs DXF output as long as the dimensions are correct and clearly labeled.
3. CAD files using metric units are preferred. All Tecdia machines run off of metric units so drawings received in standard units must be redrawn and converted. During conversion critical

dimensions can be changed so converted files must be reviewed for accuracy and approved by the customer before use.

4. To create any structure, zero width polylines that create closed polygons are required.
5. Avoid overlapping/double structures or protruding lines, as this will lead to file conversion errors and uncertain interpretation of the CAD design.
6. All drawings must be drawn in a two dimensional (2D). One 2D drawing is preferred for each surface with patterned metallization. Drawing for each surface may be in the same file, but must be clearly labeled.
7. When unclear, metallized areas should be shaded or cross-hatched to indicate where metal is.
8. Data or features that are not part of the thin film design should be removed or placed on a separate, reference only layer.
9. Tolerance for all critical dimensions should be specified within the drawing.
10. Please give each design feature a separate layer. Possible design features include, but are not limited to.
  - Substrate Outline/ Chip Outline
  - Gold Pattern (A,B,C and D Surface on separate layers)
  - Laser machining (Vias and Cut outs)
  - Thin Film Resistors (TaN)
  - AuSn Pre-Deposited Solder
  - Solder Barrier (Pt)
  - Solder Dam (Pt)
  - Bridges
11. For each design feature, please include all required information as explained in each section.

## Section 4: Substrate Material

### 4.1: Material Properties

All materials Tecdia processes are polished. There are two types of substrates materials that Tecdia processes regularly, Alumina ( $\text{Al}_2\text{O}_3$ ) and Aluminum Nitride (AlN).

Table 4.1.1: Material Properties

	$\text{Al}_2\text{O}_3$ 99.6% Polished	AlN 170 W/m*K Polished
Surface Roughness [ $\mu\text{m Ra Max.}$ ]	0.025 (Polished)	0.051 (Polished)
Dissipation Factor @ 1MHz	0.0001	0.001
Dielectric Constant [k]	9.9	9.0
Thermal Conductivity [W/m*K]	30	170
Thermal Expansion [ $10^{-6}/^\circ\text{C}$ ]	20~300°C: 7 20~600°C: 7.2	20~300°C: 4.7 20~600°C: 5.2

Additional available materials include AlN 200 W/m\*K, AlN 230 W/m\*K,  $\text{Al}_2\text{O}_3$  96%, Glass, Sapphire, BTO & STO (Titanates), Fused Silica/Quartz. Please inquire for details regarding these materials.

### 4.2: Substrate Thickness Availability

Available wafer sizes and thicknesses for each material are given in Table 4.2.1.

Table 4.2.1:  $\text{Al}_2\text{O}_3$  and AlN Available Thicknesses

Substrate Size	Standard Thicknesses	Min and Max
2"□	0.254 ± 0.0127 mm 0.381 ± 0.0127 mm 0.635 ± 0.0127 mm	Min: 0.1 ± 0.0127 mm Max: 3 mm ± 10%
4.5"□	0.635 ± 0.0127 mm	Min: 0.635 ± 0.0127 mm Max: 3 mm ± 10%

Wafers thinner than the recommended minimum thickness above can result in substrate warping and cracking which results in lower yields and increased pattern tolerance.

Standard chip dimension:

L:0.25mm~10.0mm × W:0.25mm~10.0mm × T:0.1~3.0mm

Any chip size dimension between 0.25mm~40mm is acceptable as long as the following criteria is met.

- Thickness cannot be greater than Length or Width
- Aspect Ratio between Length and Width cannot be greater than 10.

## Section 5: Conductor Layer

### 5.1: Metallization layer

The basic metallization scheme for thin film substrates contains Titanium (Ti), Platinum (Pt) and Gold (Au). This metallization stack is a “fit all” solution since it is optimal for high throughput, cost sensitive, high frequency/data rate and solder or epoxy attach applications.

Table 5.1.1: Available Metallization

Metal	Standard Thickness	Possible Range
Ti	0.06 μm	0.03 ~ 0.1 μm
Pt	0.15 μm	0.05 ~ 0.3 μm
Au	1 μm	0.1 ~ 5 μm

※Please contact Tecdia regarding metals and thicknesses outside of range given in table.

### 5.2: Conductor Pattern Tolerances

For all designs as gold increases maintaining tight tolerances and small features becomes more difficult. Minimum and standard feature limits are given in table 5.2.1 and 5.2.2 for AB and AC designs.

Fig 5.2.1: Conductor Tolerances on AB Designs

Au Thickness	Standard Line and Space	Minimum Line and Space	Standard Feature Tolerance*	Min Feature Tolerance*
≤2 μm	10 μm	5 μm	±10 μm	±5 μm
2~5 μm	20 μm	10 μm	±10 μm	±5 μm
>5 μm	20 μm	15 μm	±25 μm	±5 μm

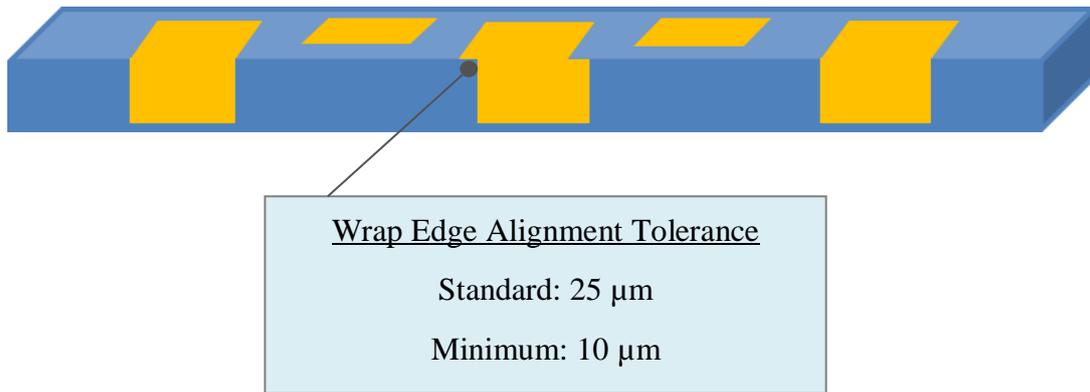
Fig 5.2.2: Conductor Tolerances on AC Designs

Au Thickness	Standard Line and Space	Minimum Line and Space	Standard Feature Tolerance*	Min Feature Tolerance*
≤2 μm	25 μm	10 μm	±15 μm	±10 μm
2~5 μm	25 μm	20 μm	±15 μm	±15 μm
>5 μm	25 μm	20 μm	±25 μm	±15 μm

\*Tolerance only applies to dimensions measured from “Feature to Feature”. Dimensions measured from feature to substrate edge must include dicing tolerance. Chip edge to pattern tolerance is 25um Min

When conductors are connected on two different surfaces, such as an AC wrap design, an extra alignment tolerance must be considered.

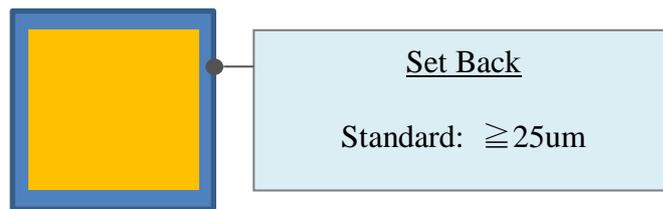
Fig 5.2.1: Conductor Tolerances on Wrapped Edge



### 5.3: Set Backs and Trace to Edge Circuits

During the substrate sawing process, there is a significant possibility that the substrate metallization will peel if the saw goes through a metallized portion of the circuit. Therefore, a metallization setback should be left between the metal trace and the edge of the circuit whenever possible.

Fig 5.3.1: Conductor Pattern Tolerances on Wrapped Surface



On wrapped substrates the traces to edge circuits on the C side are difficult to create due to limitations in resist control on bars. Therefore C side substrates should also maintain a setback between the edge of the C and B side whenever possible. The Setback rules also apply to A, B and D sides with metallization patterns applied.

Fig 5.3.2: Conductor Pattern Tolerances on Wrapped Surface



## 5.4: Multiple Surface Conductor Patterns

Beyond AB and AC patterned substrates, many possible configurations of patterned and fully metallized surfaces in a single design can exist. Table 5.4.1 gives all possible configurations with current Tecdia process.

Fig 5.4.1: Metallization Configurations

		Patterned Surface				
		0	1	2	3	4
Fully Metallized Surface	0	OK	OK	OK	Coming Soon	X
	1	OK	OK	Coming Soon	X	
	2	OK	Coming Soon	Coming Soon		
	3	OK	Coming Soon			
	4	OK				

\* Requires review before these configurations can be accepted with Pre-deposited solder layer.

Double Sided pattern AB circuit feature can be realized easily, but maintaining critical dimensions on both sides can be a challenge. Minimum Front to Back Tolerance for patterns is  $\pm 5\mu\text{m}$ .

## 5.5: Other Design Tips

### Avoid Acute Angles

In the mask creation process, the patterns are formed on the mask using rectangular flashes of light. Certain patterns, especially acute angles, require numerous flashes to form. This can result in over exposure which creates bleeding in these areas of the mask.

### Avoid Circular Structures

Circular and round structures cannot keep tight tolerances when compared to straight features with right angles. To keep processing time and cost down, it's best to avoid circular structures when possible.

### Keep Gold Thickness Constant Throughout All surfaces

Having areas of the electrode where the gold thickness is different requires extra lithography and etching processes. The extra steps and defects that occur during the extra steps add unnecessary cost and so varied gold thickness should be avoided when possible.

## Section 6: Resistor Layer

### 6.1: Available Resistor Layers

The resistors formed at Tecdia are normally formed from Tantalum Nitride (TaN) in one of three standard sheet resistivity layers as described in Table 6.1.1.

Table 6.1.1: Available Resistor Layers

TaN $\Omega/\square$ Value
25 $\Omega/\square$
50 $\Omega/\square$
75 $\Omega/\square$
100 $\Omega/\square$

Tecdia resistor layers maintain characteristics given in Table 6.1.2

Table 6.1.1: Resistor Layer Characteristics

Temperature Coefficient of Resistance	-100 $\pm$ 50ppm (-55 $\sim$ 125 $^{\circ}$ C)
Thermal Life Test	125 $^{\circ}$ C , 1000 hours Max change in resistance still under evaluation

### 6.2: Power Dissipation

No definitive studies have been performed to test the long-term reliability of the resistors built at Tecdia. Instead the below table gives figures that are commonly accepted in the thin film industry. There are a lot of parameters that will affect the power rating so if your circuit has poor heat sinking use the more conservative value, while conversely, circuits with good heat sinks can use the least conservative numbers.

Fig 6.2.1: Power Dissipation by Area

Most Conservative (Mil Spec and Space Applications)	50 Watts per square inch
Typical	400 Watts per square inch
Least Conservative	1200 Watts per square inch

\* Above table does not represent Teccia measured values

## Section 7: Pre-Deposited Solder Layer

### 7.1: Available Solder Layers

Pre-Deposited Solder Pads are formed from AuSn through an electroplating process with characteristics given in Table 7.1.1.

Table 7.1.1: Plated AuSn Specs

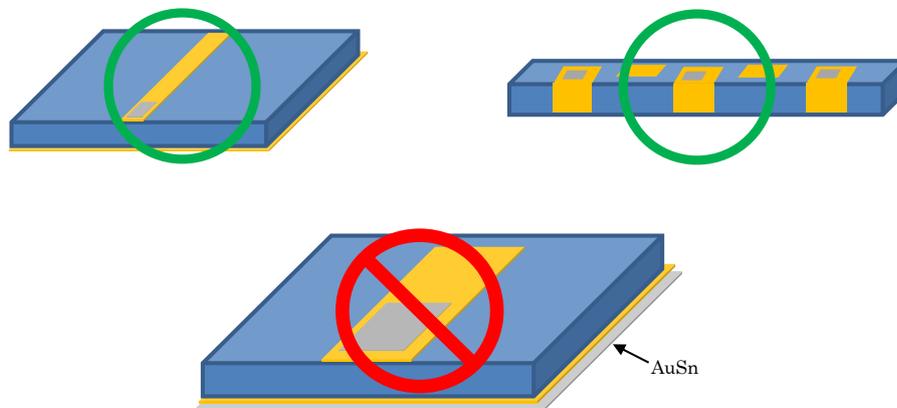
AuSn Ratio	Au 80%; Sn 20%, Au 70%; Sn 30%
AuSn Ratio Tolerance	±10%(TBD)
Thickness Range	3~7 µm (5 µm Standard)
Thickness Tolerance	± 1µm(3~4 µm), ±2 µm (4.1~7 µm)
Reflow Temperature	320°C

All solder pads sit on top of a conductor layer.

### 7.2: Solder Pad Design

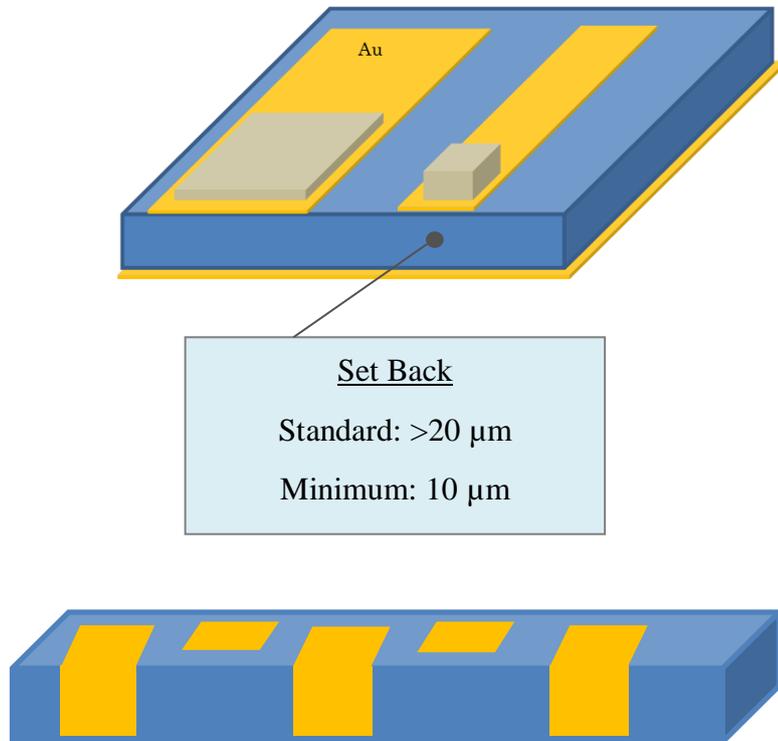
AuSn Pre-deposited solder can be applied to a single side of either flat or wrapped designs.

Fig 6.2.1: Available Resistor Configurations



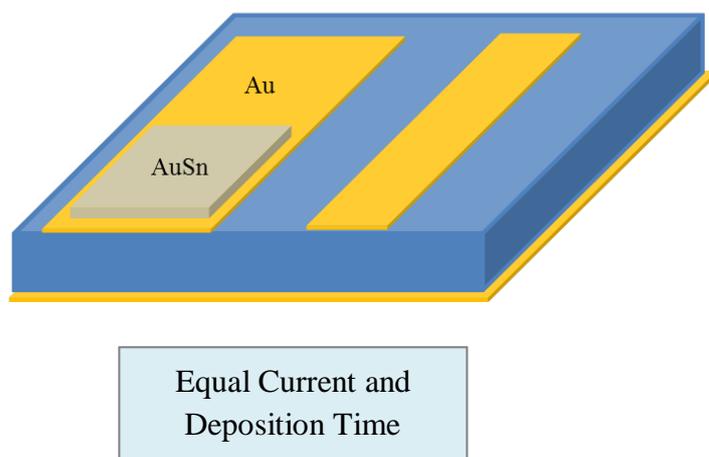
All solder pads sit on top of the conductor layer. To avoid problems with small misalignments between the gold and solder patterns the solder pads need to have a setback as seen in Fig. 7.2.1

Fig 7.2.1: AuSn Gold Set Back



Electroplated AuSn deposits as a function of current and area. When solder pads on the same surface have great variance in area it is very difficult to control the thickness for both pads. In cases where solder pad thickness is critical, electrodes with different areas should be avoided.

Fig 7.2.1: AuSn Gold Set Back



### 7.3: AuSn Solder Die Attach General Criteria

- a. Preheat components to within 150 to 200°C of the eutectic temperature of the solder pad material before performing die attach.
- b. Solder pad should be same dimensions as the bottom electrode of the component, with thickness sufficient to insure proper attachment.
- c. Typically, die-attach processing should be done under an atmosphere of  $H_2/N_2$  forming gas, 90 to 95 %  $N_2$  with 5 to 10 %  $H_2$ . (Hydrogen serves a reducing agent for thin surface oxides.)
- d. With the solder pad in its molten state, quickly place the die on the preform (if not done before) and scrub it lightly with tweezers for 2 to 3 seconds.
- e. After attaching die, remove the assembly from the die-attaching station and allow it to cool gradually.
- f. Solder attach is strongest when performed on fully metalized electrodes containing Pt barrier layer.
- g. Teccia  $Al_2O_3$  substrates with sputtered and plated metallization can withstand high temperature (400°C) die-attach conditions without physical damage for most metal stacks. Teccia  $AlN$  substrates with sputtered and plated metallization can withstand high temperature (400°C) die-attach conditions without physical damage as long as the Au thickness is  $2\mu m \pm 20\%$  or less.

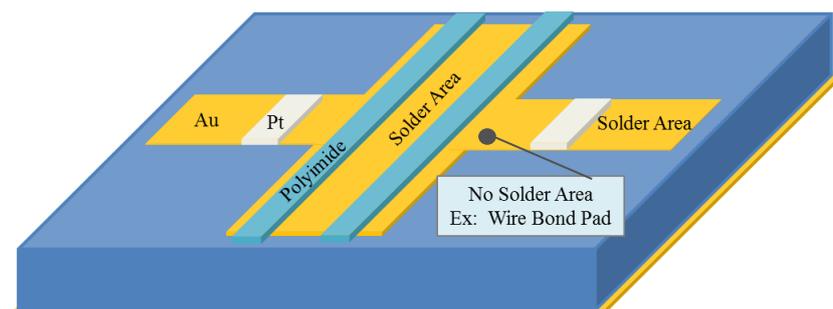
### 7.4: Solder Dam

Solder Dams are barriers that prevent solder from flowing into unwanted area. There are numerous dielectrics and metals that can be applied to create solder dams. Teccia Solder dams are normally formed using Platinum or Polyimide.

Pt Solder Dam Thickness: TBD

Fig 7.4.1: Solder Dam

## Section 8: Screening and Reliability



## 8.1: Production Screening

Tecdia performs the screening on its substrates as given in table 8.1.1 when applicable.

Table 8.1.1: Substrate Screening

Test	Test Criteria	Sampling Quantity	Applicable Designs
Visual Inspection	MIL-STD-883, Method 2032, Class H	MIL-STD-105E level II Normal 1.0%	All Designs
Wire Bond Pull	Pull Strength : $\geq 5g$ of force, Wire diameter : 25 $\mu$ m	A side only  1pcs / Lot or Monitor chip	Any Design with Conductor Layer
Heat Resistance Test	400°C for 5 minutes (Alumina) 300°C for 5 minutes (AlN) Substrates with AuSn : TBD	1pcs / Lot or Monitor chip	Any Design with Conductor Layer
Metallization Thickness	-	3pcs / Lot or Monitor chip	Any Design with Conductor Layer
Chip Dimensions	-	3pcs / Lot or Monitor chip	All Designs
Substrate Thickness	-	3pc / Lot	All Designs

## 8.2: Lot Definition

Lot numbers are assigned using the following steps

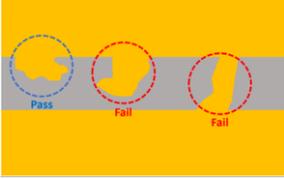
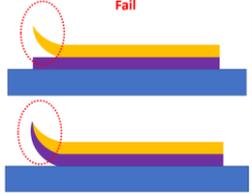
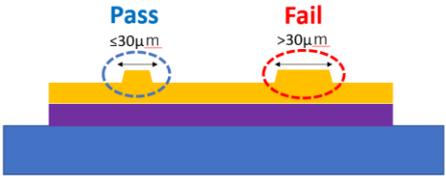
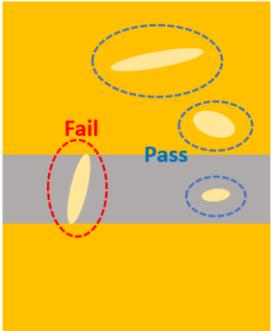
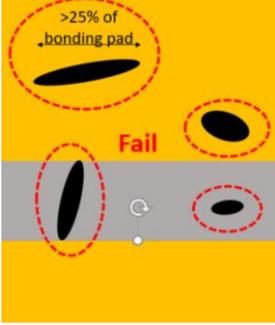
1. Lot number is assigned to parts A side sputtered together
2. Multiple part numbers cannot be sputtered together
3. All processes proceeding A side sputter cannot have mixed lots

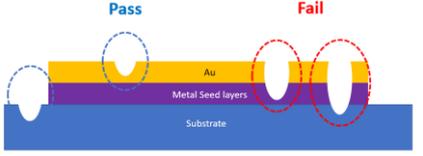
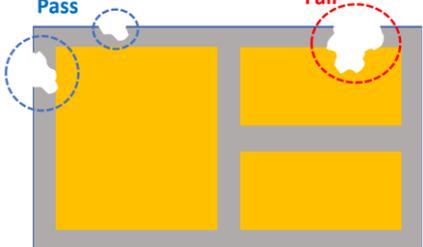
\*For internal traceability an additional internal lot number is assigned to every 10 sticks plated together.

## 8.2: Standard Visual Inspection Criteria

Inspection Standard: Mil-STD-105E Level II Normal 1%

Microscope at 20X, only inspect metallized areas

Inspection Item	Acceptance Criteria	Example
<p><u>Excess Metallization</u> Residual Metallization in gap region.</p>	<p>■ Not allowed if it reduces the original separation between adjacent patterns by 50% or more</p>	
<p><u>Metallization Deficit</u> A deficit in the designed pattern metallization</p>	<p>■ Not allowed if larger than 50% of metallization width for most traces</p>	
<p><u>Peeling Metallization</u> Peeling of metallization exposing non-Au layers or sapphire</p>	<p>■ Not Allowed</p>	
<p><u>Metallization Defect</u> Au protruding from metallization surface</p>	<p>■ Not allowed if diameter is over 30 μm</p>	
<p><u>Adhered Foreign Metal</u> Any adhered metal other than Au</p>	<p>■ Not allowed if connecting critical areas</p>	
<p><u>Adhered Foreign Contamination</u> Any non-metal contamination</p>	<p>■ Not allowed</p>	

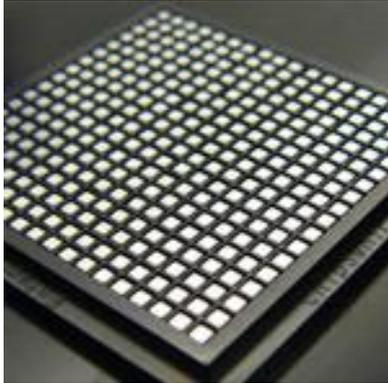
<p><u>Pattern Offset</u> Misalignment between connecting pattern on wrap edge</p>	<p>■ Not allowed if offset is greater than 25µm</p>	
<p><u>Scratch</u> Any adhered material other than Au</p>	<p>■Scratches exposing underlayer not allowed.</p>	
<p><u>Crack</u> Crack in sapphire, epitaxy, metallization or passivation.</p>	<p>■ Not allowed</p>	
<p><u>Chipping</u> Missing fragments of chip broke off during singulation.</p>	<p>■ Not allowed if chipping extends under the pattern. Chipping just touching the pattern is allowed.</p>	
<p><u>Discoloration</u> Abnormal Color caused by residual chemicals and contamination</p>	<p>■ Not allowed</p>	

\* Visual Inspection Criteria can be customized per customer request.

## Section 9: Packaging

### 9.1: Package Types and Availability

Waffle Pack



Blue Tape



Waffle packs are available for all substrate configurations. Blue Tape Packaging availability depends on chip please consult Teccia personnel for blue tape options.

Substrates on Blue Tape cannot exceed 1.2mm in Length of Width due to inspection limitations.

### 9.2: Blue Tape Packaging Specifications

Chips placed on blue tape can be shifted and rotated within the limited defined in Fig and Table 9.2.1.

Fig 9.2.1: Blue Tape Chip Alignment

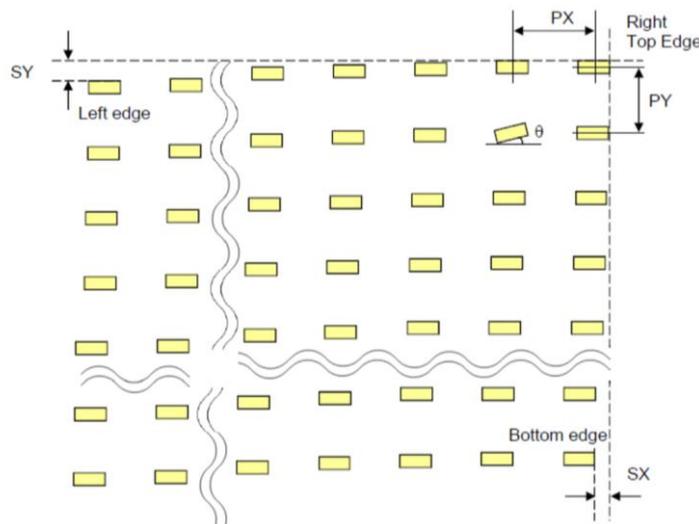


Table 9.2.1: Blue Tape Chip Alignment

Acronym		Standard Value
PX	Distance between chips (X Axis)	$\pm 0.10$ mm
PY	Distance between chips (Y Axis)	$\pm 0.10$ mm
SX	Distance between chip and Edge (X Axis)	0.40 mm MAX
SY	Distance between chip and Edge (Y Axis)	0.40 mm MAX
$\theta$	Chip rotation angle vs. X axis	$\pm 10^\circ$ MAX

Blue Tape sheet and alignment are come shipped as shown in Fig and Table 9.2.2.

Fig 9.2.2: Tape Alignment Area

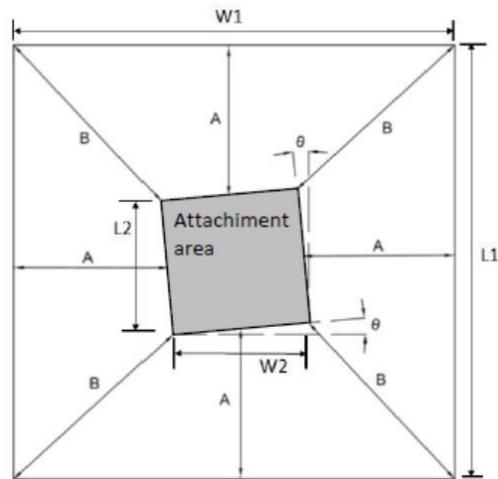
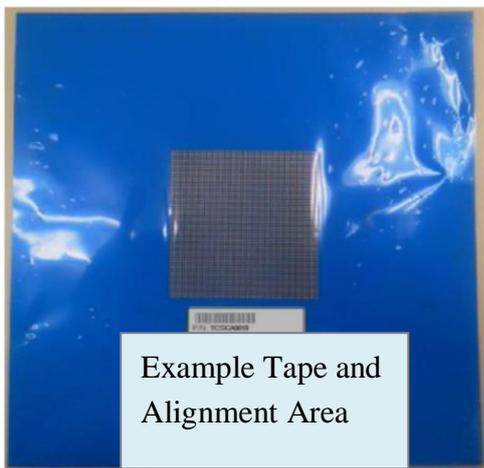
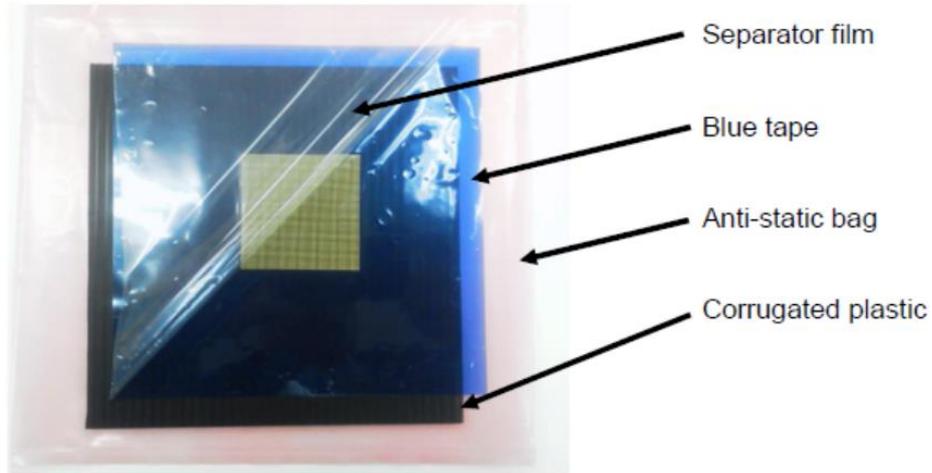


Table 9.2.2: Tape Alignment Area

Acronym		Standard Value
<b>L1</b>	Length of Entire Blue Tape Package	$200 \pm 5$ mm
<b>W1</b>	Width of Entire Blue Tape Package	$200 \pm 5$ mm
<b>L2</b>	Length of Alignment area	Max 70mm $\pm 0.5$ mm
<b>W2</b>	Width of Alignment area	Max 70mm $\pm 0.5$ mm
<b>A</b>	Alignment Area to Tape Edge	60 mm Min
<b>B</b>	Alignment Area to Tape Corner	90 mm Min
$\theta$	Alignment Area rotation angle vs. X axis	$\pm 10^\circ$ MAX

### 9.3: Blue Tape Packaging Material

Blue Tape parts are packaged and shipped as shown in Fig 9.3.1.



Tecdia packaging is compliant with EU Packaging and Packaging Waste directive for package materials (Blue tape)

Drafted by Daniel Young

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